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Proceedings of SPIE—The International Society for Optical Engineering

Volume 632

Electron-Beam, X-Ray, & Ion-Beam Techniques for Submicrometer Lithographies V

Phillip D. Blais
Chairman/Editor

11-12 March 1986
Santa Clara, California

Published by
SPIE—The International Society for Optical Engineering
P.O. Box 10, Bellingham, Washington 98227-0010 USA
Telephone 206/676-3290 (Pacific Time) • Telex 46-7053

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Please use the following format to cite material from this book:

Author(s), "Title of Paper," *Electron-Beam, X-Ray, & Ion-Beam Techniques for Submicrometer Lithographies V,* Phillip D. Blais, Editor, Proc. SPIE 632, page numbers (1986).

Library of Congress Catalog Card No. 86-061034
ISBN 0-89252-667-X

Printed in the United States of America.

Sub-micron Pattern Inspection System using Electron Beam

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Abstract

The experimental Electron Beam Inspection System (EBIS) which is used for sub-micron patterns of VLSI circuits is developed and described here. This system is designed to investigate algorithms, which extract defects, and various characteristics to use the electron beam (EB). Following will be mentioned : the configuration of EBIS, description of hardwares and softwares, considerations about pattern alignment, and algorithm extracting defects using the EB.

Introduction

As patterns of VLSI devices have been becoming smaller and more complex, the pattern inspection technology has become more important in the roll of both development and reliable production of the VLSI. It is forecasted that the 4M D-RAM will be in volume production by 1990. At this time submicron fabrication technology will be fully applied in its production[1]. Lithography technology will be improved beyond optical exposure to that of charged beams and X-rays. CD measurement technologies of patterns fabricated on in-process wafers are required to be of high resolution and repeatability. The systems for CD measurement using low-energy EB are now available and will be used in volume production[2]. An inspection system which has a higher resolution in submicron dimension than the conventional optical system will be desired. Especially the patterns, which are fabricated by EB direct writing techniques, and the patterns of 1X mask such as X-ray mask will need for precise inspection. Future trends in lithography, measurement, and inspection technologies are shown in Table 1. For future use, the submicron pattern inspection system with the EB is beig experimentally developed.

System concept

Optical pattern inspection system are now commercially available. There is however limitation in their sensitivity and resolution with optical lithography technologies. The advantages of using an EB probe are the ability to obtain a high resolution and the inherently great depth of focus, and the controllability to locate EB probe to certain fields of patterns. Because of the last fact, the distortion correction of the EB probe, and the alignments between two pattern images can be easily performed. Table 2 shows the characteristics using the EB.

There are three kinds of defects which lower device yield in VLSI production : systematic, random and repeating defects. Systematic defects, characterized by line-width variations or edge roughness, are caused by process failures such as under exposure, over developing or poor etching tolerances. Random defects, such as pinholes or intrusions, are caused by various elements of mask production process or wafer process. Repeating defects are caused by the stepper with defective reticle.

Three kinds of methods using optical technologies have been proposed[3]. They are (1) pattern-to-pattern comparison, (2) pattern-to-data comparison (3) feature extraction. Table 3 shows certain merits and limitation about these methods. The pattern-to-pattern comparison method needs precise positioning and complex hardware. In addition, repeating defects cannot be detected with this method when wafer patterns are exposed by one-die-reticle. The feature extraction method does not need precise positioning, but it needs an absolute criterion of defect recognition, so there is the possibility of missing certain types of defects. The system described here basically uses a method that compares the actual pattern with the inspection data generated from design data to detect systematic, random, and repeating defects.

System configuration

The EBIS is made up of the low-energy scanning electron microscope (LSEM), pattern generator (PG), wave form storage (WFS), the microprocessor which controls PG and WFS, digital image processor (DIP) with frame memories, and host computer. Figure 1 shows the entire EBIS system.

The LSEM is designed for general usage. LaB6 filament is used and intermediate extracting electrode, for high-brightness at low accelerating voltage, is mounted on it. Two secondary electron detectors and one backscatter electron detector are also mounted on it.

The PG, which was designed for the focused ion beam (FIB) system[4], has been modified for EBIS. It drives beam deflection/blanking electrodes of LSEM and generates timing signal for A/D conversion in WFS and DIP. The block diagram of PG is shown in Fig.2. A 16-bit microprocessor receives scan parameters, such as, scanning speed, beam positioning, scan start/end point, and deflection gain/rotation from a host computer and sets them to the digital circuits. Scanning speed can be varied from 1KHz to 20MHz. Scan generator circuit generates digital scan signals from the start point to the end point and scan DAC converts to analog signals. The gain and rotation of the deflections for each axis are corrected in order to adjust the writing field to the sample coordinate areas.

The WFS, which consists of an 8-bit A/D converter, a 16-bit adder and a high speed 16-bit line memory, is mounted to detect fidutial mark locations. The block diagram of WFS is presented in Fig.3. The one dimensional wave form signal from LSEM's detectors is converted to digital value and stored. To improve signal-to-noise (S/N) ratio, additional averaging can be performed upto 32 times by hardware. After storing the wave form this data is transferred to the microprocessor with the direct-memory-access (DMA) mode. The microprocessor then calculates the mark locations from wave form data and sends to the host computer.

The DIP is made up of an 8-bit A/D converter, an arithmetical logical unit (ALU) which can perform various operations between frame memories, multiple frame memories for storing images and inspection data, D/A converters and monitoring unit, some multiplexer circuits for selecting data path, I/F circuits to the host computer, and a control processor. The block diagram of the DIP is indicated in Fig.4. The capacity of one unit of frame memory is 1024 X 512 pixels X 8-bit. At image acquisition, two units (1024 X 1024 pixels) are used simultaneously. The signal from LSEM's detectors is converted to 8-bit digital value and stored in frame memory of 1024 X 1024 pixels. Sampling rate can be varied in accordance with the timing signal from PG. When the field of view is 100μm□ , the pixel size is about 0.1μm. On the other hand at data processing, one unit is used in a single ALU-cycle. It takes 33msec to process one unit in a single ALU-cycle. The inspection data is transferred from the host computer via the I/F circuit with DMA mode.

The host computer is a 16-bit mini-computer (DEC PDP-11/23) which controls the whole system. It also has the I/F unit connected to the CAD system in order to transfer inspection data.

Software functions

Some software shown in Fig.5 has been developed for the host computer and microprocessor in this system.

Before image acquisition, the scanning area on the sample must be adjusted to the viewing field. For this purpose, the distortion correction program is developed. The fidutial mark detection technologies are used in this program[5]. This program is divided into two parts, one for the controller of PG and WFS, the other for the host computer (refer to Fig.1). Wave forms are sampled and the location of marks are calculated by the first part. The distortion and the correction of the pre-setted gain/rotation value are calculated from these locations by the second part of the program.

Inspection data is converted from CAD data. Inspection data is a row of primitive figures, which are expressed by its vertices, such as rectangles and trapezoids. The figures in CAD data are divided into primitives and sorted into scanning fields. The array of primitive figures in one scanning field are compressed in order to inspect the large volume memory patterns.

The inspection program is a procedure of sub-functions shown in Fig.5. In order to match the actual pattern image and inspection data, mark detection and beam positioning are executed first. Image acquisition is performed by setting parameters for the DIP and starting EB probe scanning, which is driven by the PG. Image enhancement of actual patterns is done using the matrix convolution function in the DIP. The conventional smoothing matrix is selected in this time. Inspection data is read from disk storage and loaded to the frame memory. Finally, the comparison between the processed pattern image and the inspection data is executed.

Distortion correction

The viewing field was defined and adjusted to 102.4µm in this experiment. This means that the pixel size in the frame memories represents 0.1µm. The array of fidutial marks for the distortion correction were exposed by the Varian Ee-BES 40 system and fabricated on the same inspected sample. The shape of marks was cross-type, 4µm in width, and 25µm in length. 5X5 marks with 25µm pitch were located. These locations were measured by self-measuring functions which Ee-BES has, and the deviation of the differences from design was under 0.06µm. The distortion of the viewing field was measured using this system and software after gain/rotation corrections. These results are shown in Fig.6 (a). Note that the measured locations of marks (solid line) were drawn to scale 0.473µm/div. The deviation of the differences from design was 0.125µm. Figure 6(b) shows the repeatability of measurements and its deviation was 0.07µm. From these results, it is revealed that the viewing field can be adjusted within ±1 pixel error.

Image Acquisition

The example of image acquisition is indicated in Fig.7. The sample consists of resist patterns without metal coating on $MoSi_2$ glass wafer. 5KV of accelerating voltage was selected and the beam current of 1nA was used. Submicron defects are shown in Fig.7.

Inspection Algorithm

The inspection using EB has a troublesome problem: charging phenomena. The variation of image signal from the patterns on the insulating substrate does not depend upon the specific position in the field, but depends on the arrangement of patterns. In order to eliminate the variation of signal level, the edge-detection-method using spatial differentiation is considered. This procedure and its results are shown in Fig.8. The photographs in Fig.8 show the example of the Au X-Ray mask. If the signal level of pattern image varies, the conventional thresholding operation cannot be used. The edges, however, are extracted sufficiently using the operation mentioned above. Inspection data are read from disk, loaded on the frame memory, and the edges are extracted. After subtraction, the defects are detected.

Conclusion

A submicron inspection system using the EB is experimentally developed and described here. In order to match between the actual image and inspection data, it is found that the distortion of deflection can be suppressed to within +1 pixel error. The edge-detection-method using spatial differentiation is revealed to be a good procedure for detecting defects in the existence of signal level variation. For practical usage, a high throught put and a system automation will be required. After these refinements, this system will be a true sub-micron pattern inspection system.

Acknowledgments

The authors are pleased to thank Dr. H.Nakada for his great help and encouragement during the course of this study.

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		1986	1987	1988	1989	1990 ----	1995
D-RAM		256K		1M		4M	16M
Critical Dimension (μm)		1.5	1.2	1.0	0.8	0.7	0.5
Lithography	Optical		Projection and Stepper			Excimer Laser + Multi-Resist	
X-Ray	P. Source	Projection		X-Ray Stepper		High Bright Pulse	
	SOR		Experiment			Production	
EB	Mask		5X Reticle + $MoSi_2$			X-Ray Mask	
	Wafer					Direct Writing	
FIB	Mask		Photo Mask Repair			X-Ray Mask Production & Repair	
	Wafer		GaAs (Lithography)			Si (Implantation)	
Measurement & Inspection	Mask		Optical (5X Reticle)			EB (X-Ray,Excimer Laser)	
	Wafer	Optical		EB			

Table 1 Future Trends

advantages	daisadvantages
· high resolution · great depth of focus · controllability	· high cost using vacuum system · damage to devices · charging phoenomena

Table 2 Characteristics using EB Probe

methods	advantages	disadvantages
(die to die) pattern to pattern	· high throurhput	· needs precise positioning · can not detect repeating defects
(die to data base) pattern to data	· reference to CAD data	· needs precise posisioning · complex data handling
feature extraction	· need not positioning	· possibilyty of missing certain types

Table 3 Characterization of Inspection Methods

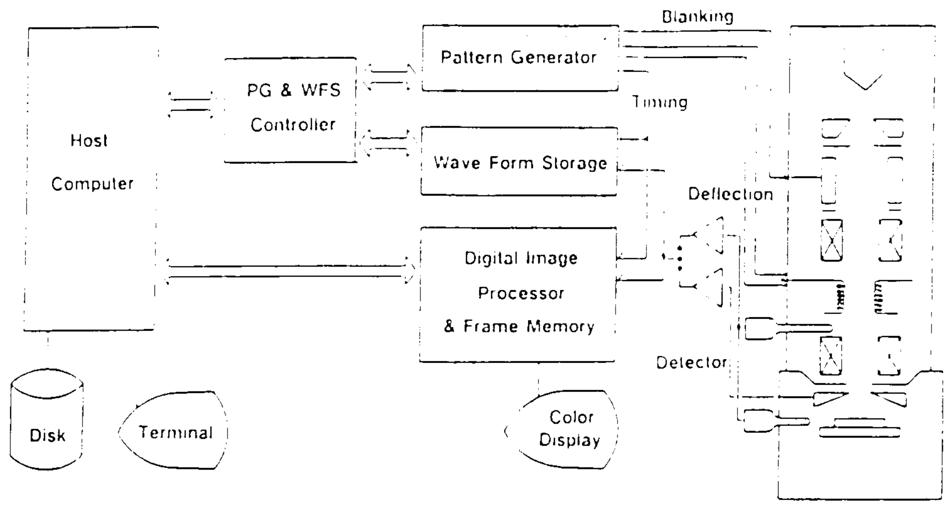


Figure 1   Configuration of EBIS

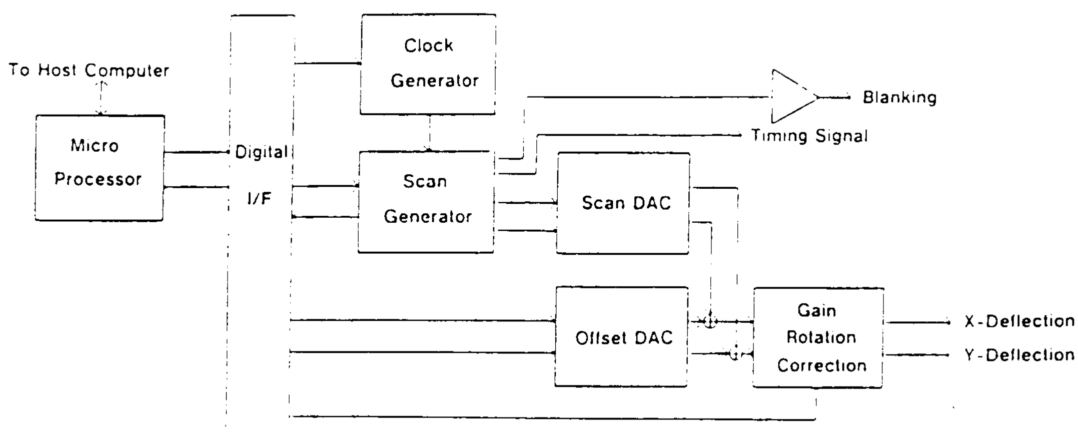


Figure 2   Block Diagram of Pattern Generator

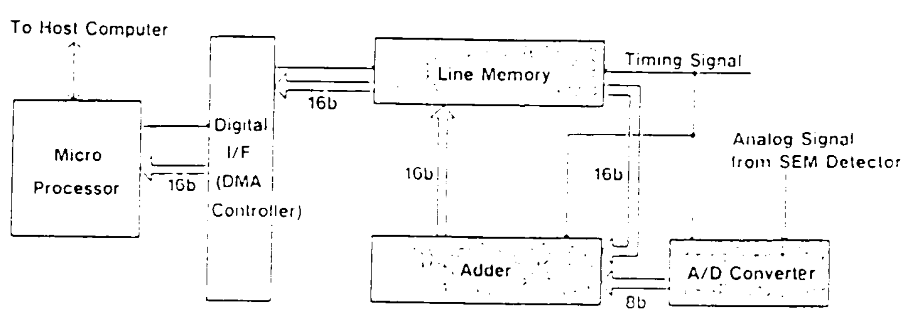


Figure 3   Block Diagram of Wave Form Strage

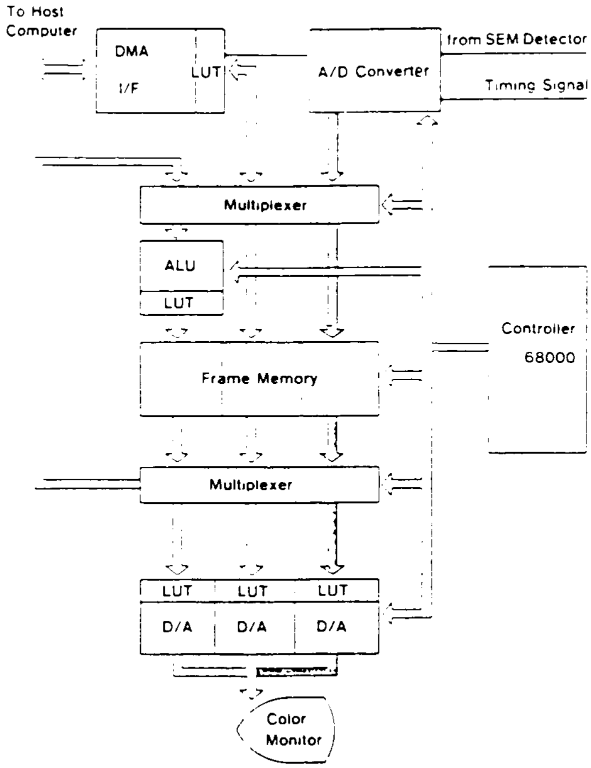


Figure 4 Block Diagram of DIP

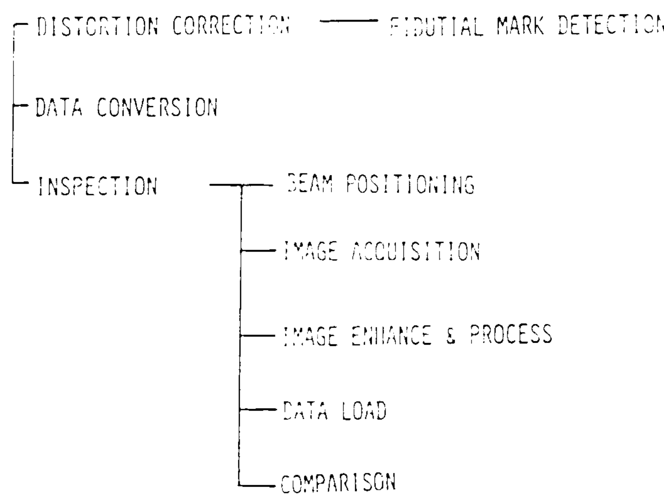
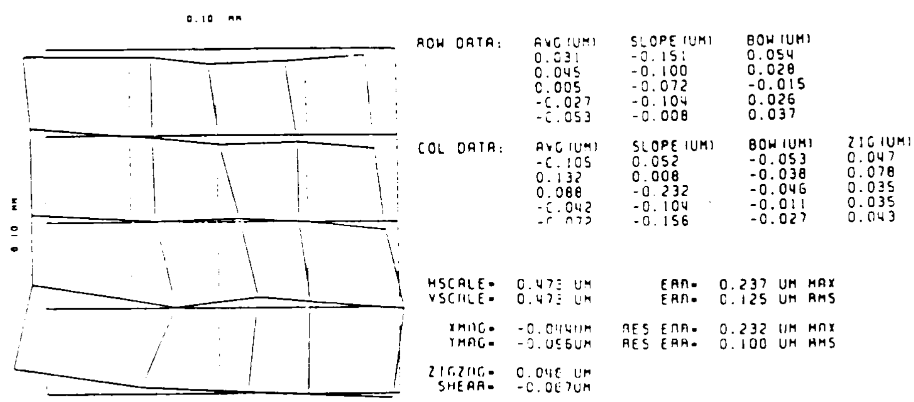


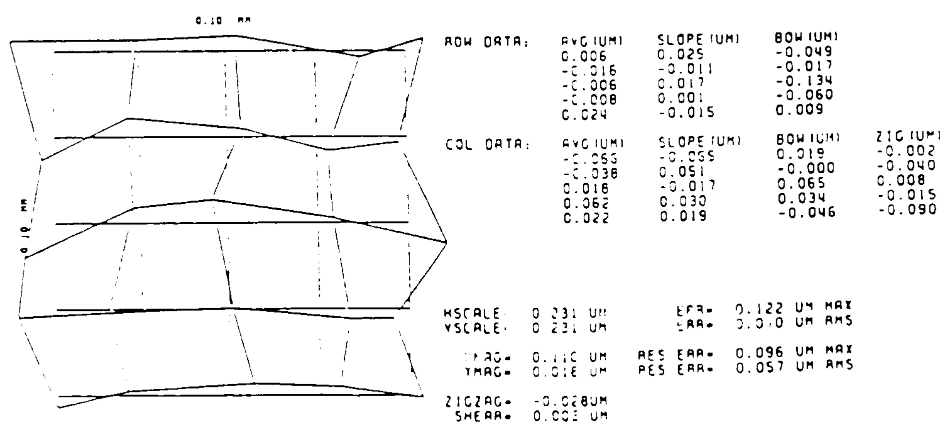
Figure 5 Software-functions of EBIS

Figure 6 Accuracy of EBIS's Deflection

(a) Distortion



(b) Repeatability



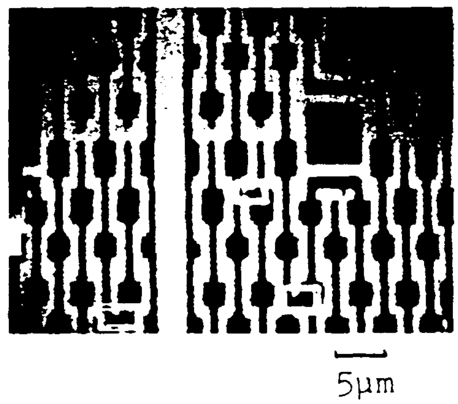


Figure 7 Example after Image Acquisition

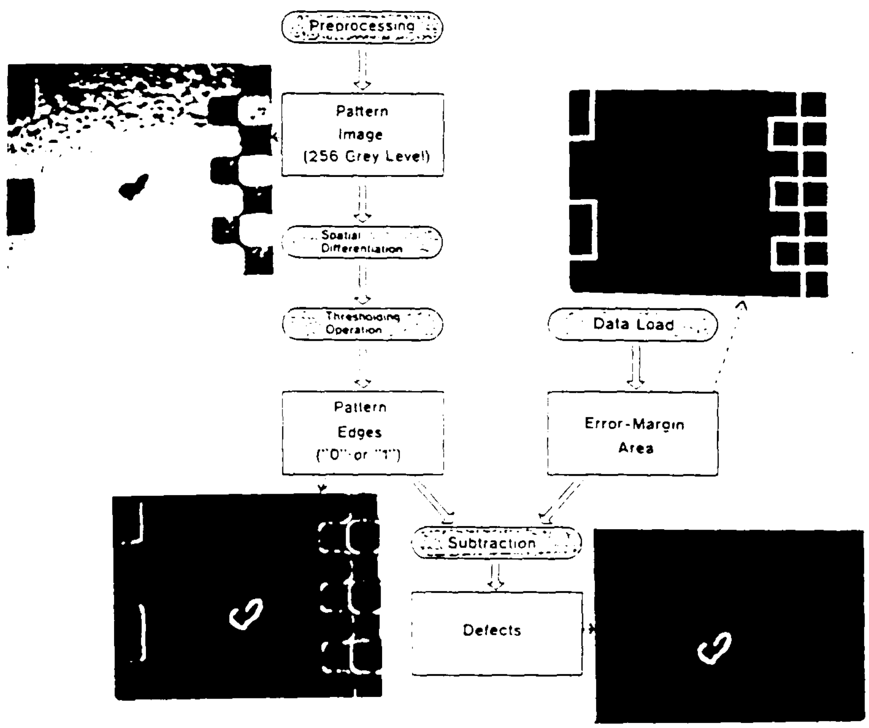


Figure 8 Procedure of Edge-detection-method